Google Web Images Groups News Froogle Local[New!] more »
simulink matlab vhdl (testbench OR "test bench" Search Advanced Search Preferences

Web Results **1 - 100** of about **757** for **simulink matlab vhdl (testbench OR "test bench")**. (**0.46** seconds)

Getting Started
... Initializing the Simulator for a **MATLAB Test Bench** Session Applying ... **Bench** Session Modeling and Verifying a **VHDL** Design with **Simulink** Overview Creating a ...
www.mathworks.com/access/helpdesk/ help/toolbox/modelsim/modelsim_tocframe.html - 18k - Feb 15, 2005 - Cached - Similar pages

[PDF] Link for ModelSim 1.1 Datasheet
File Format: PDF/Adobe Acrobat - View as HTML
... code communicates with **MATLAB** and **Simulink** through the **VHDL** wrapper and Link for ModelSim, enabling you to perform cosimulation, software **test bench**- ing ...
www.mathworks.com/mason/tag/ proxy.html?dataid=4465&fileid=20586 - Similar pages
[More results from www.mathworks.com]

DSP Builder
... system; Automatically generates a **VHDL testbench** or Quartus II Vector File (.vec) from **MATLAB** and **Simulink** test vectors; Automatically ...
www.altera.com/products/software/ products/dsp/dsp-builder.html - 31k - Cached - Similar pages

[PDF] Stratix Filtering Reference Design, Application Note 245
File Format: PDF/Adobe Acrobat - View as HTML
... Exercise 2: Simulate the Model in **Simulink** ... A **MATLAB** plot displays the frequency response of the filtered ... Turn on the Generate Stimuli for **VHDL Testbench** option ...
www.altera.com/literature/an/an245.pdf - Similar pages
[More results from www.altera.com]

[PDF] **Simulink/Matlab**-to-**VHDL** Route for Full-Custom/FPGA Rapid ...
File Format: PDF/Adobe Acrobat
... converting the **Simulink** TM design into **VHDL** has been ... **Matlab** DSP Conference (DSP'99), Tampere, Finland, 16-17 ... termination blocks (new feature in **Simulink** TM 3 ...
dolphin.wmin.ac.uk/~artur/pdf/Paper18.pdf - Similar pages

adaptyv signal processing dsp
... **Matlab** scripts demonstrating test vector generation and **testbench** output qualification ...
adaptyv.com/doc/papers/paper18.pdf **Simulink matlab VHDL** FPGA prototyping ...
www.adaptyv.com/en/links2.php?kw1=FPGA - 30k - Cached - Similar pages

adaptyv signal processing dsp
... from The MathWorks is a full-featured version of **MATLAB** and includes **Simulink** with model ... Includes **VHDL** behavioral models, a **VHDL testbench** as well as a bit ...
www.adaptyv.com/en/links2.php?kw1=**matlab** - 53k - Cached - Similar pages
[More results from www.adaptyv.com]

[PDF] Modeling and Implementation of DSP FPGA Solutions
File Format: PDF/Adobe Acrobat - View as HTML
... Core Generator Synthesizer Control Design FPGA Place & Route Logic Simulator **Simulink** **Matlab** Environment Core Parameters **VHDL** Test Vectors EDIF EDIF + Timing ...
www.xilinx-china.com/products/ logicore/dsp/**matlab**_final.pdf - Similar pages

[PDF] System Level Tools for DSP in FPGAs
File Format: PDF/Adobe Acrobat - View as HTML

... systems, as well as **MATLAB's** capabilities for ... the system model simulated in **Simulink** mirrors the generated hardware circuit, a **VHDL testbench** is automatically ...
www.xilinx-china.com/products/ logicore/dsp/sysgen_fpl2001.pdf - Similar pages
[More results from www.xilinx-china.com]

[PDF] Microsoft PowerPoint - tutorial1.1.5 br.ppt
File Format: PDF/Adobe Acrobat - View as HTML
... First start **Matlab**, then type "**simulink**" in the ... Check the "Create **Testbench**" box to enable **VHDL testbench** generation FPGA System Clock Period ...
bwrc.eecs.berkeley.edu/Research/BEE/BEE1/ doc/designflow/tutorials/tutorial1.1.5_handout_br.pdf - Similar pages

BJgroup Design Environment Support
... Next, a **Simulink** model is created and test vectors ... Lastly, the Synopsys **VHDL**-Debugger will be run to ... and assumes that the executables mc, **matlab**, vhdlan, and ...
bwrc.eecs.berkeley.edu/Research/IC_Design_Flow/ Flow/function/tut/**vhdl**simtut/default.html - 25k - Cached - Similar pages
[More results from bwrc.eecs.berkeley.edu]

Aldec - Support - Article
... to produce their spectra is implemented in **VHDL** as below: ... After initializing simulation in **SimulinkÂ®**, the results can ... in the Scope window in **MatlabÂ®** below ...
support.aldec.com/.../KnowledgeBase/ Article.aspx?aid=000262 - 74k - Cached - Similar pages

[PDF] Implementing DSP Designs with the Xilinx System Generator and ...
File Format: PDF/Adobe Acrobat
Using the Mathworks **Matlab** and **Simulink**, along with ... a plug-in to the **Simulink** modeling software ... and automatically generates a synthesizable **VHDL** code including ...
www.synplicity.com/literature/syndicated/pdf/DSP.pdf - Similar pages

[PDF] In this issue... Synplify ASIC:A Productivity Tool for ASIC ...
File Format: PDF/Adobe Acrobat - View as HTML
... Using the Mathworks **Matlab** and **Simulink**, along with ... As a plug-in to the **Simulink** modeling software ... automatically generates a synthe- sizable **VHDL** code including ...
www.synplicity.com/literature/ syndicated/pdf/Syndicated_2.pdf - Similar pages

[PDF] Specification and Algorithm/Architecture Specification and ...
File Format: PDF/Adobe Acrobat - View as HTML
... **Matlab/Simulink** interface generation **Matlab/Simulink** interface generation ... of **testbench testbench** in **Matlab** in **Matlab** ... (**VHDL**, SystemC RTL/Behav./2.0, **Matlab** ...
www.artist-embedded.org/PastEvents/ Rome04/Tuesday/ETP-Rome04-Rosenstiel-SpeAC.pdf - Similar pages

Discrete Time Compiler Users' Guide
... are added at the top level of the **Simulink** model. ... you used to test the function in **MATLAB**, simply adding ... the stimulus and translate it to **VHDL**, providing reuse ...
www.hardwarecompilers.com/users_guide/dtc_ug_test_s.htm - 10k - Cached - Similar pages

Discrete Time Compiler Users' Guide
... If the DTC option 'Add **Simulink Test Bench**' is set, and the **MATLAB** variable 'dtc_simin ... of course you want System Generator to build a **VHDL** test bed in ...
www.hardwarecompilers.com/users_guide/dtc_ug_known.htm - 19k - Cached - Similar pages
[More results from www.hardwarecompilers.com]

Importing **Matlab/Simulink** models into VCC
... with ISS (Instruction Set Simulators) and **VHDL**/Verilog simulators ... **Matlab/Simulink Testbench** in VCC. ... by imperative languages such as **Matlab/Simulink** or C code. ...
www.parades.rm.cnr.it/projects/ **matlab**vcc/whitepapers/SimulinkVCChtml.htm - 48k - Cached - Similar pages

[PDF] Filter Design HDL Coder 1
File Format: PDF/Adobe Acrobat - View as HTML
... use the generated ModelSim **test bench** to cosimulate ... Cosimulate and verify **VHDL** and Verilog using ... **MATLAB**, **Simulink**, Stateflow, Handle Graphics, and Real-Time ...
www.techsource.co.th/images/ products/download/FDHDL_Codr.pdf - Similar pages

[PDF] Microsoft PowerPoint - MUG2003_AltDo.ppt
File Format: PDF/Adobe Acrobat - View as HTML
... Solution Combining **VHDL** controller model and **Matlab/Simulink** vehicle model Restrictions of the **VHDL-testbench** Simulator Coupling Page 22. ...
www.eas.iis.fhg.de/publications/ papers/2003/034/slides.pdf - Similar pages

[PDF] Reconfigurable Logic for Hyperspectral Image Processing: Program ...
File Format: PDF/Adobe Acrobat - View as HTML
... Input **Simulink** ... **MATLAB** Environment ... Synthesis System Generator Code Generation Software • Map to IP Libraries • Control Signals • **VHDL** Design • HDL ...
klabs.org/richcontent/MAPLDCon02/ presentations/session_d/d6_coxe_s.pdf - Similar pages

[PDF] Creating Parameterized and Energy-Efficient System Generator ...
File Format: PDF/Adobe Acrobat - View as HTML
... these tools usually support automatical **testbench** genera- tion ... level design environment built on top of **MATLAB/Simulink**. ... IP cores, designs in **VHDL** or Verilog ...
klabs.org/richcontent/MAPLDCon03/papers/b/b7_ou_p.pdf - Similar pages
[More results from klabs.org]

[PDF] AN 362: Stratix II Filtering Reference Design Lab
File Format: PDF/Adobe Acrobat - View as HTML
... A **MATLAB** plot displays the frequency response of the filtered ... script, tb_filter_design. tcl, and a **VHDL testbench** that imports the **Simulink** input stimuli ...
www.altera.co.jp/literature/an/an362.pdf - Similar pages

[PDF] Stratix DSP Kit Modem Reference Design Lab Application Note
File Format: PDF/Adobe Acrobat
... perform algorithmic design and system integration in the **MATLAB** and **Simulink** ... Builder, you can also automatically generate from **Simulink** a **testbench** that you ...
www.altera.co.jp/literature/an/an281.pdf - Similar pages
[More results from www.altera.co.jp]

[PDF] Transformation of **Simulink** Models into Synthesizable HDL ...
File Format: PDF/Adobe Acrobat - View as HTML
... We reserve all rights of disposal such as copying and passing on to third parties. HDL Generation from **Simulink** Models **Matlab** Program RT Components **VHDL** ...
speac.fzi.de/WORKSHOP2/MEDEA_DATE.pdf - Similar pages

[PDF] Mastertitelformat bearbeiten
File Format: PDF/Adobe Acrobat - View as HTML
... Availability of © **Matlab** model ... Setup of a **Simulink-VHDL** cosimulation environment started: ò Next Steps ... Elaboration of a **testbench** concept
speac.fzi.de/WORKSHOP1/Stark.pdf - Similar pages

[PDF] HDL Design Verification Synthesis Design Verification
File Format: PDF/Adobe Acrobat - View as HTML
... Hardware expansion and mapping – Synthesizable **VHDL** with model ... ISE project generation to simplify the design flow – HDL **testbench** and test ... **MATLAB/Simulink** ...
www.ece.umn.edu/class/ee5545/handout/Week2.pdf - Similar pages

[PDF] Creating a 12 x 8 MAC Using the Xilinx System Generator

File Format: PDF/Adobe Acrobat - View as HTML
... You verified the design using **MATLAB** simulator through the **Simulink** environment and ran the System Generator token to generate **VHDL** code and the ...
www.ece.umn.edu/class/ee5545/Lab2/Lab2.pdf - Similar pages

[PDF] AN 245: Stratix DSP Kit Filtering Reference Design Lab
File Format: PDF/Adobe Acrobat - View as HTML
... 1. Run the **MATLAB** software. ... Figure 12. **Simulink** Design for Exercise 3 ... 6. Click the **Testbench** tab. 7. Turn on the Generate Stimuli for **VHDL Testbench** option. ...
www.altera.com.cn/literature/an/an245.pdf - Similar pages

[PDF] DSP Builder User Guide
File Format: PDF/Adobe Acrobat - View as HTML
... of a DSP system ■ Automatically generates a **VHDL** or Verilog HDL **testbench** or Quartus II Vector File (.vec) from **MATLAB** and **Simulink** test vectors ...
www.altera.com.cn/literature/ug/ug_dsp_builder.pdf - Similar pages
[More results from www.altera.com.cn]

[PDF] Analog/Mixed-Signal Modeling
File Format: PDF/Adobe Acrobat - View as HTML
... Trained Engineers Universities are teaching MAST, **Simulink/MATLAB**, Verilog-A, and **VHDL**-AMS Page 24. ... AMS **Testbench** (Aptivia from Cadence is start but ...) ...
www.ics.uci.edu/~rgupta/cande/cande03/smith03.pdf - Similar pages

[PDF] SystemC: Motivation
File Format: PDF/Adobe Acrobat - View as HTML
... Silage, Rosetta, Esterel, **MATLAB/Simulink** Page 14. - 14 - ... SystemC or **MATLAB**. **MATLAB** and **VHDL**-AMS support modeling partial differential equations. ...
ls12-www.cs.uni-dortmund.de/ ~marwedel/kluwer-es-book/es-marw-2f-c.pdf - Similar pages

[PPT] PowerPoint-Präsentation
File Format: Microsoft Powerpoint 97 - View as HTML
... SystemVerilog (2). Enhanced features for describing the **testbench**. ... SpecCharts: Combination of StateCharts and **VHDL**; designed by Gajski et al. ... **MATLAB/Simulink**. ...
ls12-www.cs.uni-dortmund.de/ ~marwedel/kluwer-es-book/es-marw-2f-c.ppt - Similar pages

[PDF] **MATLAB / Simulink**
File Format: PDF/Adobe Acrobat - View as HTML
... environment allows a developer to quickly create a valid **test bench** to verify ... Integrate legacy C and **VHDL** code and create new IP in a ... DSP **MATLAB / Simulink**
www.lyrtech.com/fr/publications/ Matlab-Simulink_graphique_Bunndle_Wireless.pdf - Similar pages

[PDF] RAPID-PROTOTYPING PLATFORM FOR WIRELESSAND SDR DEVELOPERS MORE TO ...
File Format: PDF/Adobe Acrobat - View as HTML
... allows a developer to quickly create a valid **test bench** to verify ... FPGAs ■ Access advanced IP blocks and program FPGAs without writing **VHDL** ... **MATLAB / Simulink**
www.lyrtech.com/fr/publications/ Wireless_bundle_spread.pdf - Similar pages
[More results from www.lyrtech.com]

MicroLab - I3S CAD Exercises
... of the Black-Jack dealer project; Ex451 : **Test bench** design in **VHDL** for the ... Interfacing **Matlab/Simulink** with GECKO Main Board: Advanced Exercises: Ex550 ...
www.microlab.ch/cad_ex/e.html - 18k - Cached - Similar pages

Ex 551 step1
... emulate the ports in your **test bench** and do ... Design your structural MyMotor **VHDL**;

Analyze your encoder ... exercise Ex550 for the communication with **Matlab/Simulink**. ...
www.microlab.ch/cad_ex/5sem/ex551/ex_1.htm - 24k - Cached - Similar pages
[More results from www.microlab.ch]

The Challenges of Modern FPGA Design Verification
... Then there is the important task of convincing **Matlab's Simulink** that the **VHDL** descriptions are ready for co-simulation. ...
www.fpgajournal.com/articles/20040727_aldec.htm - 27k - Cached - Similar pages

[PDF] Link for ModelSim
File Format: PDF/Adobe Acrobat - View as HTML
... **Test Bench** Function ... ます。Verilog によるコ・シミュレーショ ンも、**VHDL** ラッパーに Verilog ... Verilog コ ードは **MATLAB/Simulink** と **VHDL** ...
www.cybernet.co.jp/**matlab**/product/ general/modelsim/Link_for_ModelSim.pdf - Similar pages

FPGA FAQ comp.arch.fpga archives - messages from 71900
... easy to re-define the variable in **Matlab** which will ... you will need to do timing simulations outside of **Simulink**. ... file is then read in by a **VHDL testbench** so the ...
www.fpga-faq.com/archives/71900.html - 67k - Cached - Similar pages

FPGA FAQ comp.arch.fpga archives - messages from 64050
... because they are necessary to install **matlab/simulink** xilinx dsp ... Article: 64071 Subject: Re: **VHDL-Testbench**-Simulation in QuartusII ... A **VHDL Test Bench** File is ...
www.fpga-faq.com/archives/64050.html - 53k - Cached - Similar pages
[More results from www.fpga-faq.com]

[PDF] Automatic Conversion of **MatLab/Simulink** Models to HDL Models ...
File Format: PDF/Adobe Acrobat - View as HTML
... Changing the output HDL language, (Verilog or **VHDL**) does not affect the ... **MatLab/Simulink** ... **MatLab** offers the **test-bench**, so the implementation engineer does not ...
www.fcd.co.il/doc/optim2004.pdf - Similar pages

[PDF] WW - - CDMA CDMA real real - - time algorithm time algorithm ...
File Format: PDF/Adobe Acrobat - View as HTML
... sFunction_host.dll **matlab**.exe ubs_demo.mdl ... send results from DSP to **Simulink** measured. ... Development environment (DSP / **VHDL** code and **testbench**) proven. Page 18. ...
cmc.rice.edu/research/theses/JON2000APR4WCDMAREALT.pdf - Similar pages

Embedded News - MathWorks, Mentor Provide System Co-Simulation ...
... Manchester Receiver implemented in **VHDL** and simulated in ModelSim. ... System engineers use **MATLAB** and **Simulink** to create behavioral models of hardware systems ...
www.embeddedstar.com/press/ content/2003/10/embedded11138.html - 13k - Cached - Similar pages

Embedded News - Mentor Graphics Unveils Scalable Verification ...
... and emerging design languages -- Verilog 2001, **VHDL**, SystemVerilog (first ... between The MathWorks industry-leading products, **Simulink®** and **MATLAB®**, and a ...
www.embeddedstar.com/press/ content/2003/10/embedded11144.html - 25k - Cached - Similar pages

Product
... **MATLAB-VHDL** Á[ao]ï·ÂÕæ°Í¿ÉÊÓÐÔ. µäÐÍÓ¦ÓÃ Ê¹ÓÃ Link ... ÄÊµÀýµ Ä¿[a]·¢¡ 1 £°¿ÉÒÔÔÚ **MATLAB** »ò **Simulink** ÖÐÕë¶Ô ...
www.hirain.com/Product/module_detail. asp?menucolr=3&name=MATLAB&idd=157&id=1 - 34k - Cached - Similar pages

Research and Coursework
... level implementation was done on **MATLAB** - **Simulink** to validate ... Download ( ) We converted

the **simulink** implentation into a ... of three .vhd files) **VHDL** code for ...
ece.iisc.ernet.in/~ganesh/Research_and_Coursework.html - 20k - Cached - Similar pages

[PDF] Processes and Experiences in **VHDL** Top Down Design
File Format: PDF/Adobe Acrobat - View as HTML
... **MATLAB Simulink** graph ... **MATLAB** ... This method of **VHDL** modeling was investigated first as part of the demonstration teams tasks of validating a hardware architecture ...
www.eda.org/rassp/documents/ sanders/**vhdl**-top-down-design.pdf - Similar pages

[PDF] (Microsoft PowerPoint - AccelChip\255ProductOverview10_28_04.ppt)
File Format: PDF/Adobe Acrobat - View as HTML
... Supported with **Simulink** Blocksets ... hand RTL coding without optimizing the generated **VHDL** and without ... provide direct path to hardware for complex **MATLAB** built-in ...
www.accelchip.com/files/ AccelChip_ProductOverview10_28_04.pdf - Similar pages

[PDF] Slide 1
File Format: PDF/Adobe Acrobat - View as HTML
... **MATLAB** to **VHDL** or Verilog...automatically. Page 5. ... **MATLAB** and **Simulink** are registered trademarks of The MathWorks, Inc. ...
www.accelchip.com/files/newsletters/Issue%20Four.pdf - Similar pages

[PDF] P Dolphin .indd > PDF
File Format: PDF/Adobe Acrobat - View as HTML
... netlist (VC HSPICE) • User's guide • Virtual **Testbench** (**VHDL**/Verilog) • Functional ... **VHDL** ... TM harmonic balance for HF/RF extensions • **Simulink** TM for ...
www.dolphin.fr/pdf/dolphin-catalog.pdf - Similar pages

[PDF] Intelectual Property Modules Evaluation
File Format: PDF/Adobe Acrobat - View as HTML
... **MATLAB** I/O used to create interfaces between blocks ... of the XSG is invoked from **Simulink** and provides ... This interface translates the model to **VHDL** code and ...
www.ep.liu.se/exjobb/itn/2001/ed/002/exjobb.pdf - Similar pages

[PDF] FPGA based RF control
File Format: PDF/Adobe Acrobat - View as HTML
... Figure 2 Xilinx blockset for **Matlab/Simulink** ... All blocks can be simulated in **Simulink**. ... for the target FPGA family • **VHDL testbench** • Synthesis scripts for ...
tesla.desy.de/new_pages/TESLA_Reports/ 2003/pdf_files/tesla2003-16.pdf - Similar pages

[PPT] 31611 Real Time Signal Processing
File Format: Microsoft Powerpoint 97 - View as HTML
... Use syntax close to C. Validate against possible **simulink** model. ... Write in C on PC. Validate against **Matlab** (use mex files). ... For FPGAs: Rewrite all code in **VHDL**. ...
www.oersted.dtu.dk/31611/Plan/lecture_1.ppt - Similar pages

FPGA Tools Target Higher Levels of Abstraction | RTC Magazine
... Blocks developed with **Matlab** can be stitched together in **Simulink** or brought ... the Xilinx System Generator for DSP generates optimized **VHDL** code and IP ...
www.rtcmagazine.com/home/printthis.php?id=100125 - 16k - Cached - Similar pages

Solutions FPGA - CADvision, Solutions & Services en CAO ... - [Translate this page]
... simulador, que soporta las normas **VHDL**, Verilog y ... Pueden así en un bloque **TestBench** (a menudo ... El interfaz **Simulink** - **MatLab** El nuevo interfaz **Simulink** permite ...
www.cadvision.fr/activeHDL-es.htm - 39k - Cached - Similar pages

[PDF] Nouveautés...
File Format: PDF/Adobe Acrobat - View as HTML

... utile dans le développement de **testbench** avancé ... Memory View dans les conceptions **VHDL** et Verilog ... Interface **Simulink Matlab** All L'interface **Simulink®** permet ...
www.cadvision.fr/download/whatsnew63francais.pdf - Similar pages
[More results from www.cadvision.fr]

Printer Friendly Version
... transfer-level (RTL) Verilog and **VHDL** models with testbenches directly from **MATLAB** and **Simulink** designs. ... evaluated, a RTL can be synthesized from **MATLAB**. ...
www.wsdmag.com/Articles/Print.cfm?ArticleID=6004 - Similar pages

HARDI: News
... Pre-compiled SystemC™ libraries, **Matlab/Simulink**, Celoxica interface ... IEEE standards for **VHDL** and Verilog ... Editors, Automatic **Testbench** Generation, Simulation ...
www.hardi.com/news/aldec_ahdl62_040105.htm - 25k - Cached - Similar pages

Mentor Graphics Announces Scalable Verification Platform
... design languages -- Verilog 2001, **VHDL**, SystemVerilog (first ... between The MathWorks industry-leading products, **Simulink**? and **MATLAB**?, and a hardware description ...
www.mentor.com/products/fpga_pld/ news/scalable_verification_platform.cfm - 39k - Cached - Similar pages

Die INFOBOX - [Translate this page]
... in Sprachen wie C, C++, SystemC, SystemVerilog, **MATLAB** oder **Simulink** ermöglichen frühe ... Unterstützung von RTL-code basiertem Debug (Verilog & **VHDL**). ...
www.mentor.com/germany/infobox/presse/2003/10sca.htm - 42k - Cached - Similar pages
[More results from www.mentor.com]

[PDF] comp.lang.**vhdl** Frequently Asked Questions And Answers (Part 3) ...
File Format: PDF/Adobe Acrobat - View as HTML
... control, use of other **Simulink** modules several ... specified models Port translation / **test bench** generation Sensitivity ... FAQ comp.lang.**vhdl** (part 3) : Products & ...
tech-www.informatik.uni-hamburg.de/ **vhdl**/doc/faq/FAQ3.pdf - Similar pages

New Features in Altera's DSP Builder Version 2.0 Deliver ...
... Builder to design the equalizer as a **Simulink** model, simulate it in **MATLAB**, and then ... to synthesize and compile the generated **VHDL** files automatically ...
www.us.design-reuse.com/news/news3451.html - 48k - Cached - Similar pages

[PDF] HJ94 HJ94 hfdst hfdst . II . II Ontwerp Ontwerp van micro- van ...
File Format: PDF/Adobe Acrobat - View as HTML
... formal behaviour = concurrently executable Models of Computation (MoC) Specs = behaviour + constraints + **testbench** (see Ch ... **Matlab-Simulink** (ODE, DE ... **VHDL**-AMS (ODE ...
www.esat.kuleuven.ac.be/~iverbauw/ Courses/HJ94/lectures/les2_2slidespp.pdf - Similar pages

[PDF] Exercise 1,2. System Design Process for a Digital Bass-Booster ...
File Format: PDF/Adobe Acrobat - View as HTML
... a complete RT-description and we can go to a **VHDL** description and ... Start up **MATLAB**. ... This opens a **SIMULINK** model containing 5 first order transfer functions with ...
www.esat.kuleuven.ac.be/~iverbauw/ Courses/HJ95/HJ95_exercise1and2.pdf - Similar pages
[More results from www.esat.kuleuven.ac.be]

[PDF] Slide 1
File Format: PDF/Adobe Acrobat - View as HTML
... The MathWorks **MATLAB** / **Simulink** DSP system modeling Vendor ... **Simulink** sinks & library functions **Simulink** sources Page 14. ... period desired Generate the **VHDL** Page 16. ...
www-bd.gsi.de/Projects/FAIR_Developments/ Beam_Position_Monitors/IT_Libera_programming_RUTK.pdf - Similar pages

[PDF] Microsoft PowerPoint - Banerjee-Tech Talk Nov. 18 2004 for ...
File Format: PDF/Adobe Acrobat - View as HTML
... **Testbench** .rdl ... **VHDL** Save 6 months ... Some related products (Logic Synthesis for ASICS, FPGAs) sold for $40K Mathworks DSP products (**MATLAB/SIMULINK**) sold for $5K ...
www.uic.edu/depts/enga/pdf_files/ Banerjee_Tech_Talk_Nov_18_2004.pdf - Similar pages

[PDF] NCO Compiler Megacore Function User Guide, v2.0.2
File Format: PDF/Adobe Acrobat - View as HTML
... GX device families ■ Support for **MATLAB** version 6.5 and **Simulink** version 5.0 ... and magnitude precision ■ Generates simulation files – **VHDL** model and ...
www.msc.rl.ac.uk/europractice/ vendors/ug_nco-compiler.pdf - Similar pages

[PDF] Reed-Solomon Compiler User Guide
File Format: PDF/Adobe Acrobat
... development, simulation, and verification capabilities of The MathWorks **MATLAB** and **Simulink** system-level design tools with **VHDL** synthesis and ...
www.msc.rl.ac.uk/europractice/ vendors/rs-compiler_ug.pdf - Similar pages
[More results from www.msc.rl.ac.uk]

SOCcentral - SOC, EDA, IP and programmable logic news and ...
... existing and emerging design languages -- Verilog 2001, **VHDL**, SystemVerilog (first ... a direct link between The MathWorks products, **Simulink** and **MATLAB**, and a ...
www.soccentral.com/results.asp?entryID=3608 - 20k - Cached - Similar pages

SOCcentral - SOC, EDA, IP and programmable logic news and ...
... and Stratix¢â GX device families; Support for **MATLAB** version 6.5 and **Simulink** version 5.0; ... Generates simulation files: **VHDL** model and **testbench**; Verilog HDL ...
www.soccentral.com/results.asp?entryID=2171 - 18k - Cached - Similar pages
[More results from www.soccentral.com]

[PDF] The following list describes some of the most important additions ...
File Format: PDF/Adobe Acrobat - View as HTML
... functionality useful in advanced **test-bench** development ... the Memory View window in **VHDL** and Verilog ... **Simulink Matlab** Interface All The **Simulink®** interface allows ...
www.logmatic.ch/cms/upload/pdf/activehdl63.pdf - Similar pages

[PDF] An Efficient Methodology and Semi-automated Flow for Design and ...
File Format: PDF/Adobe Acrobat - View as HTML
... The flow uses an efficient DSP validation environment (ie **Simulink/Matlab** environment [18]). ... Generic DSP-IP **Matlab** lines **VHDL** lines Demultiplex 6 78 ...
tima.imag.fr/sls/documents/ 029_Zergainoh_version_finale.pdf - Similar pages

[PDF] Multilanguage Codesign Using SDL and **Matlab**
File Format: PDF/Adobe Acrobat - View as HTML
... eg a gate model or a synthesizable **VHDL**) or a high ... This model acts as a **testbench** for the SDL model ... window and the right part shows the **Matlab/Simulink** windows. ...
tima.imag.fr/sls/documents/sasimi_2000.pdf - Similar pages
[More results from tima.imag.fr]

[PDF] Technology-aware automation is the key to efficient DSP design
File Format: PDF/Adobe Acrobat - View as HTML
... from algorithm development – using **MATLAB** and **Simulink** – to final ... RTL in Ver- ilog or **VHDL** and relies ... algó- rithm designers prefer the **MATLAB** devel- opment ...
www.embedded-control-europe.com/pdf/ecedec04p32.pdf - Similar pages

User Manual
... and powerful tool to generate **VHDL** code from ... of Automotive Systems Based on

MATLAB/Simulink™ (SAAEI 2002). ... **Simulink™**-based Codesign and Cosimulation of a ...
polimage.polito.it/CodeSimulink/ help/CodeSimulink/userManual.html - 20k - Cached - Similar pages

Tech Tips System Generator for DSP Getting Started
... via HDL co-simulation, or write **MATLAB** code for ... for DSP is invoked from **Simulink** through the ... Simulation/Verification - A **VHDL testbench** and data vectors can ...
www.xilinx.com/xlnx/xil_tt_gettingstarted. jsp?sProduct=sysgen&iLanguageID=1 - 27k - Cached - Similar pages

[PDF] Microsoft PowerPoint - dsp_software_video_apps
File Format: PDF/Adobe Acrobat - View as HTML
... Page 33. **MATLAB/Simulink** Page 34. ... **Simulink** to **VHDL** compiler – **Simulink** netlister ... Synthesizable **VHDL** with model hierarchy preserved – Xilinx Smart-IP ...
www.xilinx.com/esp/automotive/collateral/ Presentations/dsp_software_video_apps.pdf - Similar pages
[More results from www.xilinx.com]

Insight Electronics - FPGA-based DSP system design tool
... Data flow models, traditional hardware design languages (**VHDL** and Verilog), and ... which means the extensive tool sets that **Simulink** and **MATLAB** provide are ...
www.electronicsnews.com.au/articles/a8/0c01aea8.asp - 35k - Cached - Similar pages

Avnet Electronics Marketing -> Avnet Electronics Speedway ...
... Xilinx Spartan-3 ISE 6.1i, ISE 6.2i, **MatLab/Simulink**, System Generator ... An overview of **VHDL testbench** concepts and simulation techniques are explored through a ...
em.avnet.com/sta/home/0,4610,RID=0&CID=9067& CCD=USA&SID=4744&DID=DF2&LID=0&BID=DF... - 56k - Cached - Similar pages

[PDF] Vorlesungsunterlagen zu "Konstruktion elektronischer Ger und ...
File Format: PDF/Adobe Acrobat
... Institut für Elektronik **Matlab Matlab//Simulink Simulink** ... **VHDL** vs. **VHDL** vs. ... Institut für Elektronik Simulation (Simulation (**Testbench Testbench**)) ...
www.ife.tugraz.at/LV/kegs/Beschreibungssprachen_6pp.pdf - Similar pages

[PDF] Vorlesungsunterlagen zu "Konstruktion elektronischer Ger und ...
File Format: PDF/Adobe Acrobat
... **Matlab Matlab//Simulink Simulink** Mathematische Modellierung ... **VHDL** vs. **VHDL** vs. ... Simulation (
Simulation (**Testbench Testbench**)) **Testbench** zur Steuerung der ...
www.ife.tugraz.at/LV/kegs/Beschreibungssprachen_2pp.pdf - Similar pages

[PDF] Design of a Low Density Parity Check Iterative Decoder
File Format: PDF/Adobe Acrobat - View as HTML
... **Matlab** script ... A **VHDL testbench** was used for comparison of the two different descriptions. The **Simulink** model generated random input values and calculated the ...
www.eecs.berkeley.edu/Programs/ ugrad/superb/papers2002/nguyen.pdf - Similar pages

[PDF] Entwurfsmethodik bei FPGA's
File Format: PDF/Adobe Acrobat - View as HTML
... Mit **Simulink** und **MATLAB** kann ... eines Systems realisieren. **Simulink** bietet dem Benutzer zB auch Bibliotheken an, ... Ganz vorne ist hierbei **VHDL**. ...
www.informatik.uni-ulm.de/ni/ Lehre/SS03/ProSemFPGA/Entwurfsmethodik.pdf - Similar pages

[PDF] Online generierte **VHDL**-Module für arithmetische Operationen
File Format: PDF/Adobe Acrobat - View as HTML
... Verifikation wird **Simulink**, ein Simulationstool von **Matlab**, verwendet. ... in der Wurzelortskurve und in **Simulink** stabil, wird der Regler in **VHDL** implementiert ...
www.fh-nuernberg.de/fhn/service/03_anlaufstellen/ 02_pressestelle/pdf/meier_baesig_nr19.pdf - Similar pages

/bbs/pub/**vhdl**-ams: Re: Definition for matrices in **VHDL**-AMS
... we're working on a **VHDL**-AMS compiler to **Matlab/Simulink**. ... one dimensional real arrays are defined in **VHDL**-AMS ... USE work.Matrix.ALL; ENTITY **testbench** IS END ENTITY ...
www.**vhdl**.org/analog/hm/0046.html - 9k - Cached - Similar pages

/bbs/pub/**vhdl**-ams: Definition for matrices in **VHDL**-AMS
... working on a **VHDL**-AMS compiler to **Matlab/Simulink**. ... in the actual **VHDL**-AMS language ... abcd; ---- ENTITY **testbench** IS END ...
www.**vhdl**.org/analog/hm/0045.html - 6k - Cached - Similar pages
[More results from www.vhdl.org]

Mathworks: eg3.com electronic tearsheet
... quantized discrete-time FIR filter, generating **VHDL** code for the filter, and verifying the **VHDL** code with a ... seminar Introducing **MATLAB** 7 and **Simulink** 6: The ...
www.eg3.com/exe_tear/mathworks.htm - 14k - Cached - Similar pages

EE Times - Mentors Mixed-Signal-Tools werden vielseitiger - [Translate this page]
... jetzt auch den SpecMan Elite **Testbench** Generator von Verisity und Mathworks **Matlab Simulink** unterstützen. ... unterstützt außerdem Verilog, **VHDL**, Verilog-AMS ...
www.eetimes.de/ed/news/ showArticle.jhtml?articleID=19502629 - 30k - Cached - Similar pages

[PDF] Digital Signal Processing Algorithms-in-Silicon
File Format: PDF/Adobe Acrobat - View as HTML
... AccelChip now extends both **MATLAB** and **Simulink** flows to implementation! Page 20. ... radix FFT design from **MATLAB** to **VHDL** in days rather than weeks." ...
www.parallel-systems.co.uk/ pdf/accelchip_presentation.pdf - Similar pages

Aldec - Press Releases
... SystemCÔ libraries, **Matlab/Simulink**, Celoxica interface ... to IEEE standards for **VHDL** and Verilog ... & Schematic Editors, Automatic **Testbench** Generation, Simulation ...
www.aldec.com/Press/Releases/?ID=236&year=2004 - 34k - Cached - Similar pages

Bit Mapper - VLSI Design
... Automatic Self-checking **Test bench** Generation Using HDL Bencher. ... such as EDIF, SDF, **VHDL**, VITAL/Verilog ... FPGAs using the popular **MATLAB®/Simulink** products from ...
www.bitmapper.com/VLSILabSetup.html - 16k - Cached - Similar pages

[PDF] Programmable Logic Services – Support – Solutions
File Format: PDF/Adobe Acrobat
... interface between the Altera design software and The Mathworks **MATLAB** and **Simulink** tools for ... ModelSim-Altera Simulates HDL code using a **VHDL** or Verilog HDL ...
www.ebv.com/media.php/EBV/Franchises/ alteraboards/EBV_BROCHURE_July_2004.pdf?dl=1 - Similar pages

training
... 30.11.2005. Introduction to **Simulink**, 01.12. - 02.12.2005. DSP Flow with **MATLAB**, 05.12. ... The course will stress good coding techniques for reusable **VHDL** code. ...
www.so-logic.co.at/en/productstraining.php - 53k - Feb 16, 2005 - Cached - Similar pages

[PPT] [Sample Course Title Slide Insert Presentation Title]
File Format: Microsoft Powerpoint 97 - View as HTML
... System Generator. HDL. System Generator. **MATLAB/Simulink**. System Verification. **VHDL**. IP. **Testbench**. Constraints File. Synthesis. Implementation. Download. ...
www.cse.psu.edu/~cg478/03sp/lec/xilinx/dsp/x03flows.ppt - Similar pages

Chip Design Magazine
... In most verification environments, the **VHDL testbench** is a BFM. Therefore,

it contains many procedures that the e **testbench** would call. ...
www.chipdesignmag.com/display. php?articleId=67&issueId=7 - 61k - Cached - Similar pages

[PDF] EDUCATION
File Format: PDF/Adobe Acrobat - View as HTML
... Java, AWK, Linda, CORBA Applications: AutoCAD, **MATLAB**, PSpice, XiLinx ... s System Generator to translate the **Simulink** model into actual **VHDL** code that could ...
www.ece.neu.edu/~jnosewor/resume.pdf - Similar pages

MICROELECTRONIC SYSTEMS NEWS
... in conjunction with the popular **MATLAB/Simulink** software ... As a plug-in for the **Simulink** modeling software ... and automatically generates synthesizable **VHDL** code and ...
vlsi1.engr.utk.edu/~bouldin/ MUGSTUFF/NEWSLETTERS/DATA/9970.html - 3k - Cached - Similar pages

More speed and features for HDL designers - Aldec
... precompiled SystemC libraries, **Matlab/Simulink**, Celoxica interface ... to IEEE standards for **VHDL** and Verilog ... editors, automatic **testbench** generation, simulation ...
www.electronicstalk.com/news/axw/axw104.html - 11k - Cached - Similar pages

Rajan Konar 8555 N.Capital of TX Hwy, #2111, Austin TX78759 * 214 ...
... Innoveda) STA , Timing Designer(Chronology), **MatLab**, **Simulink**, Schematic and ... Languages: Verilog/**VHDL**, PERL, 8051 Assembly, C ... Modified the **testbench** to enable ...
www.utdallas.edu/~rpk021000/Complete_Resume.txt - 10k - Cached - Similar pages

Goooooogle ▶
Result Page: 1 2 3 4 5 **Next**

Results – powered by ProQuest® Smart Search

Suggested Topics About < Previous | Next >

- Electronic design automation
- Electronic design automation AND Integrated circuits
- Electronic design automation AND Software packages
- Electronic design automation AND Simulation

Browse Suggested Publications About < Previous | Next >

- Electronic Engineering Times; Manhasset
- EDN; Boston
- Electronic Design; Cleveland

4 documents found for: *(simulink and vhdl and matlab) AND PDN(<10/16/2001)* Set up Alert About

All sources | Trade Publications

☐ Mark / Clear all on page | View marked documents | Show all documents Sort results by: Most recent first

1. **QuickMACH Compiler Reduces Voice Over Network Design Time in QuickDSP Devices**
   Business Editors/High-Tech Writers. **Business Wire.** New York: Jun 18, 2001. p. 1
   Full text Abstract

2. **Design for system-on-a-programmable-chip**
   David Greenfield. **Electronic News.** New York: Jan 15, 2001. Vol. 47, Iss. 3; p. 34 (2 pages)
   Full text Page Image - PDF Abstract

3. **Suppliers developing highly integrated solutions**
   Carol Rosen. **ECN.** Radnor: Jul 1999. Vol. 43, Iss. 7; p. 51 (11 pages)
   Text+Graphics Page Image - PDF Abstract

4. **Altera Ships a Complete FIR Compiler Design Solution**
   Business Editors/High-Tech Writers. **Business Wire.** New York: May 10, 1999. p. 1
   Full text Abstract

1-4 of 4

Want an alert for new results sent by email? Set up Alert About Results per page: 30

Basic Search

Tools: Search Tips Browse Topics 1 Recent Searches

simulink and vhdl and matlab Search Clear

Database: Multiple databases... Select multiple databases

Date range: Before this date... 10/16/2001 About

Limit results to: ☑ Full text documents only

☐ Scholarly journals, including peer-reviewed About

More Search Options

EAST SEARCH

2/17/05

L#	Hits	Search String	Databases
L1	685	(system near4 design$5) same (hdl or vhdl)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L2	119	1 and (clock same (control and hardware))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L3	4	2 and (matlab or simulink)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L4	1	6305001.PN.	USPAT; USOCR
L5	65	2 and (output near5 port)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L6	2	5 and (sample near5 rate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

Results of search set L2:

US 20050034090 A1	Circuit designing method and a circuit designing system	20050210	716/6
US 20050030425 A1	Customizable ASIC with substantially non-customizable portion that supplies pixel data to a mask-programmable portion in multiple color space formats	20050210	348/553
US 20050022143 A1	System and method for performing design verification	20050127	716/5
US 20050010880 A1	Method and user interface for debugging an electronic system	20050113	716/4
US 20040268181 A1	Method and apparatus for unifying self-test with scan-test during prototype debug and production test	20041230	714/30
US 20040267972 A1	Configurable ATA/IDE host controller with SpeedSelect registers	20041230	710/8
US 20040250050 A1	Method and apparatus for controlling program instruction completion timing for processor verification	20041209	712/218
US 20040225977 A1	System and method for simulating clock drift between asynchronous clock domains	20041111	716/6
US 20040216080 A1	Method, system and program product for specifying and using dials having phased default values to configure a simulated or physical digital system	20041028	716/18
US 20040216079 A1	Method, system and program product for specifying a configuration of a digital system described by a hardware description language (HDL) model	20041028	716/18
US 20040216078 A1	Method, system and program product that utilize a configuration database to configure a hardware digital system having multiple access methods	20041028	716/18
US 20040216077 A1	Method, system and program product for specifying and using a dial having a default value to configure a digital system described by a hardware description language (HDL) model	20041028	716/18
US 20040216076 A1	METHOD, SYSTEM AND PROGRAM PRODUCT FOR UTILIZING A CONFIGURATION DATABASE TO CONFIGURE A HARDWARE DIGITAL SYSTEM	20041028	716/18

US 20040216075 A1	Method, system and program product for specifying a dial group for a digital system described by a hardware description language (HDL) model	20041028	716/18
US 20040216068 A1	Method, system and program product for reducing a size of a configuration database utilized to configure a hardware digital system	20041028	716/11
US 20040216008 A1	Method, system and program product for automatically transforming a configuration of a digital system utilizing traceback of signal states	20041028	714/33
US 20040215436 A1	Method, system and program product for implementing a read-only dial in a configuration database of a digital design	20041028	703/15
US 20040215435 A1	Method, system and program product for determining a configuration of a digital design by reference to an invertible configuration database	20041028	703/15
US 20040215434 A1	Method, system and program product for configuring a simulation model of a digital design	20041028	703/15
US 20040215433 A1	Method, system and program product that utilize a configuration database to configure a hardware digital system having an arbitrary system size and component set	20041028	703/14
US 20040215432 A1	Method, system and program product for specifying a configuration for multiple signal or dial instances in a digital system	20041028	703/14
US 20040194038 A1	Integrated circuit design system and method using preprocessor which changes hardware description in accordance with configuration	20040930	716/1
US 20040181385 A1	HDL Co-simulation in a high-level modeling system	20040916	703/14
US 20040172519 A1	Processor, system LSI circuit, method of designing same, and recording medium having said method recorded thereon	20040902	712/209
US 20040163072 A1	Electronic design automation with automatic generation of hardware description language (HDL) code	20040819	717/106
US 20040158697 A1	Pipelined microprocessor, apparatus, and method for performing early correction of conditional branch instruction mispredictions	20040812	712/239
US 20040158696 A1	Pipelined microprocessor, apparatus, and method for generating early status flags	20040812	712/234
US 20040153926 A1	Method and apparatus for testing asynchronous set/reset faults in a scan-based integrated circuit	20040805	714/726
US 20040145033 A1	Integrated circuit devices and methods and apparatuses for designing integrated circuit devices	20040729	257/659
US 20040045015 A1	Common interface framework for developing field programmable device based applications independent of target circuit board	20040304	719/328
US 20040025122 A1	Hardware-based HDL code coverage and design analysis	20040205	716/4
US 20040006584 A1	Array of parallel programmable processing engines and deterministic method of operating the same	20040108	718/107
US 20030216901 A1	Design apparatus and a method for generating an implementable description of a digital system	20031120	703/13

US 20030187662 A1	System, method, and article of manufacture for a reconfigurable hardware-based audio decoder	20031002	704/500
US 20030184593 A1	System, method and article of manufacture for a user interface for an MP3 audio player	20031002	715/810
US 20030182642 A1	Hardware debugging in a hardware description language	20030925	716/4
US 20030182641 A1	Rapid input/output probing apparatus and input/output probing method using the same, and mixed emulation/simulation method based on it	20030925	716/4
US 20030149962 A1	Simulation of designs using programmable processors and electronically re-configurable logic arrays	20030807	717/135
US 20030144828 A1	Hub array system and method	20030731	703/21
US 20030131325 A1	Method and user interface for debugging an electronic system	20030710	716/4
US 20030097615 A1	On-chip logic analyzer	20030522	714/37
US 20030069724 A1	Method and system for debugging an electronic system using instrumentation circuitry and a logic analyzer	20030410	703/16
US 20030066057 A1	System, method and article of manufacture for collaborative hardware design	20030403	717/140
US 20030061409 A1	System, method and article of manufacture for dynamic, automated product fulfillment for configuring a remotely located device	20030327	710/8
US 20030055771 A1	System, method and article of manufacture for a reverse-auction-based system for hardware development	20030320	705/37
US 20030055770 A1	System, method and article of manufacture for an auction-based system for hardware development	20030320	705/37
US 20030055769 A1	System, method and article of manufacture for a library-based hardware configuration service	20030320	705/37
US 20030055658 A1	System, method and article of manufacture for dynamic, automated fulfillment of an order for a hardware product	20030320	705/1
US 20030037317 A1	Method and apparatus for debugging in a massively parallel processing environment	20030220	717/129
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220	716/4
US 20030033234 A1	System, method and article of manufacture for a hardware configuration service	20030213	705/37
US 20030028408 A1	System, method and article of manufacture for a contractor-based hardware development service	20030206	705/8
US 20030023941 A1	Computer-aided design system to automate scan synthesis at register-transfer level	20030130	716/4
US 20030005392 A1	Method of designing a logic circuit	20030102	716/2
US 20020184560 A1	Multiple-capture DFT system for scan-based integrated circuits	20021205	714/25
US 20020152060 A1	Inter-chip communication system	20021017	703/17
US 20020099455 A1	Programmable controller	20020725	700/83
US 20020055834 A1	Reconfigurable test system	20020509	703/27

US 20010034876 A1	System for converting hardware designs in high-level programming languages to hardware implementations	20011025	716/18
US 6848085 B2	System for converting hardware designs in high-level programming languages to hardware implementations	20050125	716/3
US 6834360 B2	On-chip logic analyzer	20041221	714/37
US 6826732 B2	Method, system and program product for utilizing a configuration database to configure a hardware digital system	20041130	716/1
US 6823497 B2	Method and user interface for debugging an electronic system	20041123	716/4
US 6810442 B1	Memory mapping system and method	20041026	710/22
US 6785873 B1	Emulation system with multiple asynchronous clocks	20040831	716/4
US 6769122 B1	Multithreaded layered-code processor	20040727	718/102
US 6754763 B2	Multi-board connection system for use in electronic design automation	20040622	710/317
US 6701491 B1	Input/output probing apparatus and input/output probing method using the same, and mixed emulation/simulation method based on it	20040302	716/4
US 6651225 B1	Dynamic evaluation logic system and method	20031118	716/4
US 6629312 B1	Programmatic synthesis of a machine description for retargeting a compiler	20030930	717/136
US 6618839 B1	Method and system for providing an electronic system design with enhanced debugging capabilities	20030909	716/4
US 6606588 B1	Design apparatus and a method for generating an implementable description of a digital system	20030812	703/15
US 6581191 B1	Hardware debugging in a hardware description language	20030617	716/4
US 6523155 B1	Method for partitioning a netlist into multiple clock domains	20030218	716/7
US 6421808 B1	Hardware design language for the design of integrated circuits	20020716	716/1
US 6421251 B1	Array board interconnect system and method	20020716	361/788
US 6408428 B1	Automated design of processor systems using feedback from internal measurements of candidate systems	20020618	716/17
US 6389379 B1	Converification system and method	20020514	703/14
US 6324678 B1	Method and system for creating and validating low level description of electronic design	20011127	716/18
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120	716/6
US 6311149 B1	Reconfigurable test system	20011030	703/21
US 6256770 B1	Register transfer level (RTL) based scan insertion for integrated circuit design processes	20010703	716/18
US 6233540 B1	Design environment and a method for generating an implementable description of a digital system	20010515	703/14
US 6226776 B1	System for converting hardware designs in high-level programming language to hardware implementations	20010501	716/3
US 6216255 B1	Computer-aided logic circuit designing apparatus computer-aided logic circuit designing system, and computer-aided logic circuit designing method	20010410	716/6

US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic device	20010410	716/1
US 6152612 A	System and method for system level and circuit level modeling and design simulation using C++	20001128	703/23
US 6134516 A	Simulation server system and method	20001017	703/27
US 6026230 A	Memory simulation system and method	20000215	703/13
US 6021266 A	Method of designing an integrated circuit using scheduling and allocation with parallelism and handshaking communication, and an integrated circuit designed by such method	20000201	716/2
US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 5974245 A	Method and apparatus for making integrated circuits by inserting buffers into a netlist	19991026	716/10
US 5953235 A	Method for processing a hardware independent user description to generate logic circuit elements including flip-flops, latches, and three-state buffers and combinations thereof	19990914	716/18
US 5907698 A	Method and apparatus for characterizing static and dynamic operation of an architectural system	19990525	716/6
US 5870588 A	Design environment and a design method for hardware/software co-design	19990209	703/13
US 5870308 A	Method and system for creating and validating low-level description of electronic design	19990209	716/18
US 5867691 A	Synchronizing system between function blocks arranged in hierarchical structures and large scale integrated circuit using the same	19990202	713/400
US 5862149 A	Method of partitioning logic designs for automatic test pattern generation based on logical registers	19990119	714/726
US 5854926 A	Method and apparatus for identifying flip-flops in HDL descriptions of circuits without specific templates	19981229	717/156
US 5801958 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	19980901	716/18
US 5801956 A	Method for deciding the feasibility of logic circuit prior to performing logic synthesis	19980901	716/4
US 5751592 A	Apparatus and method of supporting functional design of logic circuit and apparatus and method of verifying functional design of logic circuit	19980512	716/5
US 5748488 A	Method for generating a logic circuit from a hardware independent user description using assignment conditions	19980505	716/18
US 5737574 A	Method for generating a logic circuit from a hardware independent user description using mux conditions and hardware selectors	19980407	711/162
US 5691911 A	Method for pre-processing a hardware independent description of a logic circuit	19971125	716/18

US 5684808 A	System and method for satisfying mutually exclusive gating requirements in automatic test pattern generation systems	19971104	714/726
US 5680318 A	Synthesizer for generating a logic network using a hardware independent description	19971021	716/18
US 5661661 A	Method for processing a hardware independent user description to generate logic circuit elements including flip-flops, latches, and three-state buffers and combinations thereof	19970826	716/18
US 5638291 A	Method and apparatus for making integrated circuits by inserting buffers into a netlist to control clock skew	19970610	716/18
US 5598344 A	Method and system for creating, validating, and scaling structural description of electronic device	19970128	716/18
US 5581781 A	Synthesizer for generating a logic network using a hardware independent description	19961203	716/18
US 5572436 A	Method and system for creating and validating low level description of electronic design	19961105	716/18
US 5557531 A	Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation	19960917	716/1
US 5555201 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	19960910	716/1
US 5553002 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface	19960903	716/11
US 5544066 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of low-level design constraints	19960806	716/18
US 5541849 A	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters	19960730	716/18
US 5530841 A	Method for converting a hardware independent user description of a logic circuit into hardware components	19960625	716/3
KR 2003023485 A	Device for design verification by mixing formal verification of emulation and simulation	20030319	

Full-text Search Prototype Results

Feedback Help

Your search matched **49** of **1043417** documents.
A maximum of **500** results are displayed, **50** to a page, sorted by **Publication year** in **Ascending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

simulink and vhdl and matlab Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Subject Index**

Industry Applications, IEEE Transactions on , Volume: 34 , Issue: 6 , Nov.-Dec. 1998
Pages:43 - 123

[Abstract] [PDF Full-Text (888 KB)] **IEEE JNL**

---

2 **Author Index**

Industry Applications, IEEE Transactions on , Volume: 34 , Issue: 6 , Nov.-Dec. 1998
Pages:1 - 42

[Abstract] [PDF Full-Text (676 KB)] **IEEE JNL**

---

3 **Implementation of a state space controller in a FPGA**
Garbergs, B.; Sohlberg, B.;
Electrotechnical Conference, 1998. MELECON 98., 9th Mediterranean , Volume: 1 , 18-20 May 1998
Pages:566 - 569 vol.1

[Abstract] [PDF Full-Text (256 KB)] **IEEE CNF**

---

4 **On-chip analog signal generation for mixed-signal built-in self-test**
Dufort, B.; Roberts, G.W.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 3 , March 1999
Pages:318 - 330

[Abstract] [PDF Full-Text (540 KB)] **IEEE JNL**

---

5 **Book Reviews**

Circuits and Devices Magazine, IEEE , Volume: 16 , Issue: 6 , Nov. 2000
Pages:44 - 48

[Abstract] [PDF Full-Text (108 KB)] **IEEE JNL**

---

6 **Computer-aided design of analog and mixed-signal integrated circuits**
Gielen, G.G.E.; Rutenbar, R.A.;
Proceedings of the IEEE , Volume: 88 , Issue: 12 , Dec. 2000
Pages:1825 - 1854

[Abstract] [PDF Full-Text (552 KB)] **IEEE JNL**

---

7 **System specification experiments on a common benchmark**
Gorla, G.; Moser, E.; Nebel, W.; Villar, E.;
Design & Test of Computers, IEEE , Volume: 17 , Issue: 3 , July-Sept. 2000
Pages:22 - 32

[Abstract] [PDF Full-Text (108 KB)] **IEEE JNL**

---

8 **FunState-an internal design representation for codesign**
Strehl, K.; Thiele, L.; Gries, M.; Ziegenbein, D.; Ernst, R.; Teich, J.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 4 , Aug. 2001
Pages:524 - 544

[Abstract] [PDF Full-Text (448 KB)] **IEEE JNL**

---

9 **The telecomputing laboratory: a multipurpose laboratory**
DeBrunner, V.E.; DeBrunner, L.S.; Radhakrishnan, S.; Kamal Khan, A.;
Education, IEEE Transactions on , Volume: 44 , Issue: 4 , Nov. 2001
Pages:302 - 310

[Abstract] [PDF Full-Text (65 KB)] **IEEE JNL**

---

10 **Modeling of mixed control and dataflow systems in MASCOT**
Bjureus, P.; Jantsch, A.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 5 , Oct. 2001
Pages:690 - 703

[Abstract] [PDF Full-Text (200 KB)] **IEEE JNL**

---

11 **A pipelined noise shaping coder for fractional-N frequency synthesis**
Kozak, M.; Kale, I.;
Instrumentation and Measurement, IEEE Transactions on , Volume: 50 , Issue: 5 , Oct. 2001
Pages:1154 - 1161

[Abstract] [PDF Full-Text (157 KB)] **IEEE JNL**

---

12 **Application of foresight's technology to implement a waveform development environment**
Logan, B.; Wilson, D.;
Military Communications Conference, 2001. MILCOM 2001. Communications for Network-Centric Operations: Creating the Information Force. IEEE , Volume: 1 , 28-31 Oct. 2001
Pages:218 - 224 vol.1

[Abstract] [PDF Full-Text (92 KB)] **IEEE CNF**

---

13 **Design of an optimized IC for control algorithms of AC machines: system testing and application**
Fathallah, M.; Chante, J.P.; Calmon, F.; El-husseini, M.H.;
Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE , Volume: 1 , 30 Sept.-4 Oct. 2001
Pages:103 - 109 vol.1

[Abstract] [PDF Full-Text (1312 KB)] **IEEE CNF**

---

14 **Practical considerations for a waveform development environment**
Gudaitis, M.S.; Hinman, R.D.;
Military Communications Conference, 2001. MILCOM 2001. Communications for Network-Centric Operations: Creating the Information Force. IEEE , Volume: 1 , 28-31 Oct. 2001
Pages:190 - 194 vol.1

[Abstract] [PDF Full-Text (142 KB)] **IEEE CNF**

---

15 **SPI - a system model for heterogeneously specified embedded systems**
Ziegenbein, D.; Richter, K.; Ernst, R.; Thiele, L.; Teich, J.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 4 , Aug. 2002
Pages:379 - 389

[Abstract] [PDF Full-Text (823 KB)] **IEEE JNL**

---

16 **Nanometer mixed-signal system-on-a-chip design**
Chou, E.; Sheu, B.;
Circuits and Devices Magazine, IEEE , Volume: 18 , Issue: 4 , July 2002
Pages:7 - 17

[Abstract] [PDF Full-Text (491 KB)] **IEEE JNL**

---

17 **Theoretical analysis of bus-invert coding**
Rung-Bin Lin; Chi-Ming Tsai;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 6 , Dec. 2002
Pages:929 - 934

[Abstract] [PDF Full-Text (367 KB)] **IEEE JNL**

---

18 **A methodology for system-level synthesis of mixed-signal applications**
Oehler, P.; Grimm, C.; Waldschmidt, K.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume:

10 , Issue: 6 , Dec. 2002
Pages:935 - 942

[Abstract] [PDF Full-Text (598 KB)] **IEEE JNL**

---

19 **Virtual benchmarking and model continuity in prototyping embedded multiprocessor signal processing systems**
Janka, R.S.; Wills, L.M.; Baumstark, L.B., Jr.;
Software Engineering, IEEE Transactions on , Volume: 28 , Issue: 9 , Sept. 2002
Pages:832 - 846

[Abstract] [PDF Full-Text (1097 KB)] **IEEE JNL**

---

20 **A design environment for high-throughput low-power dedicated signal processing systems**
Davis, W.R.; Zhang, N.; Camera, K.; Markovic, D.; Smilkstein, T.; Ammer, M.J.; Yeo, E.; Augsburger, S.; Nikolic, B.; Brodersen, R.W.;
Solid-State Circuits, IEEE Journal of , Volume: 37 , Issue: 3 , March 2002
Pages:420 - 431

[Abstract] [PDF Full-Text (217 KB)] **IEEE JNL**

---

21 **Lorenz chaotic model using Filed Programmable Gate Array (FPGA)**
Aseeri, M.A.; Sobhy, M.I.; Lee, P.;
Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 1 , 4-7 Aug. 2002
Pages:I - 527-30 vol.1

[Abstract] [PDF Full-Text (298 KB)] **IEEE CNF**

---

22 **A component architecture for FPGA-based, DSP system design**
Spivey, G.; Bhattacharyya, S.S.; Nakajima, K.;
Application-Specific Systems, Architectures and Processors, 2002. Proceedings. The IEEE International Conference on , 17-19 July 2002
Pages:41 - 51

[Abstract] [PDF Full-Text (371 KB)] **IEEE CNF**

---

23 **Customising floating-point designs**
Gaffar, A.A.; Luk, W.; Cheung, P.Y.K.; Shirazi, N.;
Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on , 22-24 April 2002
Pages:315 - 317

[Abstract] [PDF Full-Text (545 KB)] **IEEE CNF**

---

24 **On two new trends in evolvable hardware: employment of HDL-based structuring, and design of multi-functional circuits**
Stoica, A.; Zebulum, R.S.; Keymeulen, D.; Ferguson, M.I.; Xin Guo;
Evolvable Hardware, 2002. Proceedings. NASA/DoD Conference on , 15-18 July 2002
Pages:56 - 59

[Abstract] [PDF Full-Text (361 KB)] **IEEE CNF**

25 **From system specification to layout: seamless top-down design methods for analog and mixed-signal applications**
Sommer, R.; Rugen-Herzig, I.; Hennig, E.; Gatti, U.; Malcovati, P.; Maloberti, F.; Einwich, K.; Clauss, C.; Schwarz, P.; Noessing, G.;
Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings , 4-8 March 2002
Pages:884 - 891

[Abstract] [PDF Full-Text (632 KB)] **IEEE CNF**

---

26 **Implementation issues of neuro-fuzzy hardware: going toward HW/SW codesign**
Reyneri, L.M.;
Neural Networks, IEEE Transactions on , Volume: 14 , Issue: 1 , Jan. 2003
Pages:176 - 194

[Abstract] [PDF Full-Text (622 KB)] **IEEE JNL**

---

27 **Rapid prototyping of digital controls for power electronics**
Monti, A.; Santi, E.; Dougal, R.A.; Riva, M.;
Power Electronics, IEEE Transactions on , Volume: 18 , Issue: 3 , May 2003
Pages:915 - 923

[Abstract] [PDF Full-Text (538 KB)] **IEEE JNL**

---

28 **Wordlength optimization for linear digital signal processing**
Constantinides, G.A.; Cheung, P.Y.K.; Luk, W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 22 , Issue: 10 , Oct. 2003
Pages:1432 - 1442

[Abstract] [PDF Full-Text (650 KB)] **IEEE JNL**

---

29 **Design and testing of spacecraft power systems using VTB**
Zhenhua Jiang; Shengyi Liu; Dougal, R.A.;
Aerospace and Electronic Systems, IEEE Transactions on , Volume: 39 , Issue: 3 , July 2003
Pages:976 - 989

[Abstract] [PDF Full-Text (1984 KB)] **IEEE JNL**

---

30 **The synchronous languages 12 years later**
Benveniste, A.; Caspi, P.; Edwards, S.A.; Halbwachs, N.; Le Guernic, P.; de Simone, R.;
Proceedings of the IEEE , Volume: 91 , Issue: 1 , Jan. 2003
Pages:64 - 83

[Abstract] [PDF Full-Text (551 KB)] [Full-Text HTML] **IEEE JNL**

---

31 **Taming heterogeneity - the Ptolemy approach**
Eker, J.; Janneck, J.W.; Lee, E.A.; Jie Liu; Xiaojun Liu; Ludvig, J.; Neuendorffer, S.; Sachs, S.; Yuhong Xiong;
Proceedings of the IEEE , Volume: 91 , Issue: 1 , Jan. 2003
Pages:127 - 144

[Abstract] [PDF Full-Text (976 KB)] [Full-Text HTML] **IEEE JNL**

---

32 **Design of optimal and narrow-band Laguerre filters for sigma-delta demodulators**
Abeysekera, S.S.; Yao Xue; Charoensak, C.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 50 , Issue: 7 , July 2003
Pages:368 - 375

[Abstract] [PDF Full-Text (571 KB)] **IEEE JNL**

---

33 **Concurrent and simple digital controller of an AC/DC converter with power factor correction based on an FPGA**
de Castro, A.; Zumel, P.; Garcia, O.; Riesgo, T.; Uceda, J.;
Power Electronics, IEEE Transactions on , Volume: 18 , Issue: 1 , Jan. 2003
Pages:334 - 343

[Abstract] [PDF Full-Text (926 KB)] **IEEE JNL**

---

34 **System level specification in Lava**
Singh, S.;
Design, Automation and Test in Europe Conference and Exhibition, 2003 , 2003
Pages:370 - 375

[Abstract] [PDF Full-Text (KB)] **IEEE CNF**

---

35 **Perturbation analysis for word-length optimization**
Constantinides, G.A.;
Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , 9-11 April 2003
Pages:81 - 90

[Abstract] [PDF Full-Text (334 KB)] **IEEE CNF**

---

36 **SystemC-AMS requirements, design objectives and rationale**
Vachoux, A.; Grimm, C.; Einwich, K.;
Design, Automation and Test in Europe Conference and Exhibition, 2003 , 2003
Pages:388 - 393

[Abstract] [PDF Full-Text (KB)] **IEEE CNF**

---

37 **Future design tools for platform FPGAs**
Lysaght, P.;
Integrated Circuits and Systems Design, 2003. SBCCI 2003. Proceedings. 16th Symposium on , 8-11 Sept. 2003
Pages:275 - 280

[Abstract] [PDF Full-Text (279 KB)] **IEEE CNF**

---

38 **Accelerating bit error rate testing using a system level design tool**
Singh, V.; Root, A.; Hemphill, E.; Shirazi, N.; Hwang, J.;
Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , 9-11 April 2003

Pages:62 - 68

[Abstract] [PDF Full-Text (342 KB)] **IEEE CNF**

---

39 **The EUROPRACTICE mini@sic program**
Das, C.; McLean, J.;
Microelectronic Systems Education, 2003. Proceedings. 2003 IEEE International Conference on , 1-2 June 2003
Pages:45 - 46

[Abstract] [PDF Full-Text (211 KB)] **IEEE CNF**

---

40 **Logarithmic arithmetic for real data types and support for Matlab/Simulink based rapid-FPGA-prototyping**
Pohl, Z.; Schier, J.; Licko, M.; Hermanek, A.; Tichy, M.; Matousek, R.; Kadlec, J.;
Parallel and Distributed Processing Symposium, 2003. Proceedings. International , 22-26 April 2003
Pages:6 pp.

[Abstract] [PDF Full-Text (423 KB)] **IEEE CNF**

---

41 **A middleware for signal-flow digital simulation models in electric vehicle powertrain**
Cai Yunpeng; Sun Xiaomin; Jia Peifa;
Vehicular Technology Conference, 2003. VTC 2003-Fall. 2003 IEEE 58th , Volume: 5 , 6-9 Oct. 2003
Pages:3267 - 3271

[Abstract] [PDF Full-Text (304 KB)] **IEEE CNF**

---

42 **An efficient methodology and semi-automated flow for design and validation of complex digital signal processing ASICS macro-cells**
Tambour, L.; Zergainoh, N.; Urard, P.; Michel, H.; Jerraya, A.A.;
Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Workshop on , 9-11 June 2003
Pages:56 - 63

[Abstract] [PDF Full-Text (357 KB)] **IEEE CNF**

---

43 **Rapid design and analysis of communication systems using the BEE hardware emulation environment**
Chen Chang; Kuusilinna, K.; Richards, B.; Chen, A.; Chan, N.; Brodersen, R.W.; Nikolic, B.;
Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Workshop on , 9-11 June 2003
Pages:148 - 154

[Abstract] [PDF Full-Text (469 KB)] **IEEE CNF**

---

44 **An analytical integration method for the simulation of continuous-time /spl Delta//spl Sigma/ modulators**
Gielen, G.G.E.; Francken, K.; Martens, E.; Vogels, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 23 , Issue: 3 , March 2004
Pages:389 - 399

[Abstract] [PDF Full-Text (568 KB)] **IEEE JNL**

45 **Multiparadigm Modeling in Embedded Systems Design**
Muller-Glaser, K.D.; Frick, G.; Sax, E.; Kuhl, M.;
Control Systems Technology, IEEE Transactions on , Volume: 12 , Issue: 2 , March 2004
Pages:279 - 292

[Abstract] [PDF Full-Text (1032 KB)] **IEEE JNL**

46 **Computer-Automated Multiparadigm Modeling in Control Systems Technology**
Mosterman, P.J.; Sztipanovits, J.; Engell, S.;
Control Systems Technology, IEEE Transactions on , Volume: 12 , Issue: 2 , March 2004
Pages:223 - 234

[Abstract] [PDF Full-Text (464 KB)] **IEEE JNL**

47 **Design and behavioral modeling tools for optical network-on-chip**
Briere, M.; Carrel, L.; Michalke, T.; Mieyeville, F.; O'Connor, I.; Gaffiot, F.;
Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings , Volume: 1 , 16-20 Feb. 2004
Pages:738 - 739

[Abstract] [PDF Full-Text (211 KB)] **IEEE CNF**

48 **Design, Automation and Test in Europe Conference and Exhibition Table of Contents**

Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings , Volume: 3 , 16-20 Feb. 2004
Pages:v - ix

[PDF Full-Text (184 KB)] **IEEE CNF**

49 **A framework for low power audio design**
Vs, N.; Mertsching, B.;
VLSI Design, 2004. Proceedings. 17th International Conference on , 5-9 Jan. 2004
Pages:1048 - 1053

[Abstract] [PDF Full-Text (274 KB)] **IEEE CNF**

Full-text Search Prototype Results

Your search matched **127** of **1043417** documents.
A maximum of **500** results are displayed, **50** to a page, sorted by **Publication year** in **Ascending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

hdl and clock and control and sample and rate Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Integrated Electronics for a Reading Aid for the Blind**
Brugler, J.S.; Meindl, J.D.; Plummer, J.D.; Salsbury, P.J.; Young, W.T.;
Solid-State Circuits, IEEE Journal of , Volume: 4 , Issue: 6 , Dec 1969
Pages:304 - 312

[Abstract] [PDF Full-Text (1792 KB)] **IEEE JNL**

---

2 **Design of embedded systems: formal models, validation, and synthesis**
Edwards, S.; Lavagno, L.; Lee, E.A.; Sangiovanni-Vincentelli, A.;
Proceedings of the IEEE , Volume: 85 , Issue: 3 , March 1997
Pages:366 - 390

[Abstract] [PDF Full-Text (252 KB)] **IEEE JNL**

---

3 **Specification and analysis of timing constraints for embedded systems**
Gupta, R.K.; De Micheli, G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 3 , March 1997
Pages:240 - 256

[Abstract] [PDF Full-Text (536 KB)] **IEEE JNL**

---

4 **Embedded software in real-time signal processing systems: application and architecture trends**
Paulin, P.G.; Liem, C.; Cornero, M.; Nacabal, F.; Goossens, G.;
Proceedings of the IEEE , Volume: 85 , Issue: 3 , March 1997
Pages:419 - 435

[Abstract] [PDF Full-Text (252 KB)] **IEEE JNL**

---

5 **Integrated circuit testing for quality assurance in manufacturing: history, current status, and future trends**
Grochowski, A.; Bhattacharya, D.; Viswanathan, T.R.; Laker, K.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 44 , Issue: 8 , Aug. 1997
Pages:610 - 633

[Abstract] [PDF Full-Text (468 KB)] **IEEE JNL**

---

6 **Hardware/software co-design of digital telecommunication systems**
Bolsens, I.; De Man, H.J.; Lin, B.; Van Rompaey, K.; Vercauteren, S.; Verkest, D.;
Proceedings of the IEEE , Volume: 85 , Issue: 3 , March 1997
Pages:391 - 418

[Abstract] [PDF Full-Text (452 KB)] **IEEE JNL**

---

7 **A PAL/NTSC digital video encoder on 0.6-μm CMOS with 66 dB typical SNR, 0.4% differential gain, and 0.2° differential phase**
Cummins, T.; Murray, B.; Prendergast, C.;
Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 7 , July 1997
Pages:1091 - 1100

[Abstract] [PDF Full-Text (252 KB)] **IEEE JNL**

---

8 **1997 Index**

Photonics Technology Letters, IEEE , Volume: 9 , Issue: 12 , Dec. 1997
Pages:0_5 - 0_92

[Abstract] [PDF Full-Text (3884 KB)] **IEEE JNL**

---

9 **1997 Index IEEE Transactions On Applied Superconductivity Vol. 7**

Applied Superconductivity, IEEE Transactions on , Volume: 7 , Issue: 4 , Dec. 1997
Pages:1 - 129

[Abstract] [PDF Full-Text (5904 KB)] **IEEE JNL**

---

10 **The design of an adaptive on-line binary arithmetic-coding chip**
Shiann-Rong Kuang; Jer-Min Jou; Yuh-Lin Chen;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 45 , Issue: 7 , July 1998
Pages:693 - 706

[Abstract] [PDF Full-Text (424 KB)] **IEEE JNL**

---

11 **A 70-Mb/s variable-rate 1024-QAM cable receiver IC with integrated 10-b ADC and FEC decoder**

Loke Kun Tan; Putnam, J.S.; Fang Lu; D'Luna, L.J.; Mueller, D.W.; Kindsfater, K.R.; Cameron, K.B.; Joshi, R.B.; Hawley, R.A.; Samueli, H.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 12 , Dec. 1998
Pages:2205 - 2218

[Abstract] [PDF Full-Text (812 KB)] **IEEE JNL**

---

12 **A 3.3-V power adaptive 1244/622/155 Mbit/s transceiver for ATM, SONET/SDH**
Belot, D.; Dugoujon, L.; Dedieu, S.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 7 , July 1998
Pages:1047 - 1058

[Abstract] [PDF Full-Text (368 KB)] **IEEE JNL**

---

13 **An agile ISM band frequency synthesizer with built-in GMSK data modulation**
Filiol, N.M.; Riley, T.A.D.; Plett, C.; Copeland, M.A.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 7 , July 1998
Pages:998 - 1008

[Abstract] [PDF Full-Text (220 KB)] **IEEE JNL**

---

14 **High-level power modeling, estimation, and optimization**
Macii, E.; Pedram, M.; Somenzi, F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 11 , Nov. 1998
Pages:1061 - 1079

[Abstract] [PDF Full-Text (300 KB)] **IEEE JNL**

---

15 **A cellular analog network for MRF-based video motion detection**
Luthon, F.; Dragomirescu, D.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 46 , Issue: 2 , Feb. 1999
Pages:281 - 293

[Abstract] [PDF Full-Text (840 KB)] **IEEE JNL**

---

16 **A real-time digital VCR encode/decode and MPEG-2 decode LSI implemented on a dual-issue RISC processor**
Mohri, A.; Yamada, A.; Yoshida, Y.; Sato, H.; Takata, H.; Nakakimura, K.; Hashizume, M.; Shimotsuma, Y.; Tsuchihashi, K.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 7 , July 1999
Pages:992 - 1000

[Abstract] [PDF Full-Text (328 KB)] **IEEE JNL**

---

17 **Models for systematic design and verification of frequency synthesizers**
De Smedt, B.; Gielen, G.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 46 , Issue: 10 , Oct. 1999
Pages:1301 - 1308

[Abstract] [PDF Full-Text (140 KB)] **IEEE JNL**

18 **Pausible clocking-based heterogeneous systems**
Yun, K.Y.; Dooply, A.E.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 7 , Issue: 4 , Dec. 1999
Pages:482 - 488

[Abstract] [PDF Full-Text (316 KB)] **IEEE JNL**

19 **A 0.155-, 0.622-, and 2.488-Gb/s automatic bit-rate selecting clock and data recovery IC for bit-rate transparent SDH systems**
Scheytt, J.C.; Hanke, G.; Langmann, U.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 12 , Dec. 1999
Pages:1935 - 1943

[Abstract] [PDF Full-Text (612 KB)] **IEEE JNL**

20 **A single-chip universal cable set-top box/modem transceiver**
D'Luna, L.J.; Tan, L.K.; Mueller, D.; Laskowski, J.L.; Cameron, K.; Jind-Yeh Lee; Gee, D.; Monroe, J.S.; Law, H.S.; Chang, J.; Wakayama, M.H.; Kwan, T.; Chi-Hung Lin; Buchwald, A.; Kaylani, T.; Lu, F.; Spieker, T.; Hawley, R.; Smaueli, H.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 11 , Nov. 1999
Pages:1647 - 1660

[Abstract] [PDF Full-Text (704 KB)] **IEEE JNL**

21 **Introduction to RF simulation and its application**
Kundert, K.S.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 9 , Sept. 1999
Pages:1298 - 1319

[Abstract] [PDF Full-Text (352 KB)] **IEEE JNL**

22 **VHDL modeling and model testing for DSP applications**
Armstrong, J.R.; Gray, F.G.; Meng-Wei Lin;
Industrial Electronics, IEEE Transactions on , Volume: 46 , Issue: 1 , Feb. 1999
Pages:13 - 22

[Abstract] [PDF Full-Text (592 KB)] **IEEE JNL**

23 **A fast-search motion estimation method and its VLSI architecture**
Pei-Yin Chen; Jet Min Jou;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 46 , Issue: 9 , Sept. 1999
Pages:1233 - 1240

[Abstract] [PDF Full-Text (580 KB)] **IEEE JNL**

24 **Subject Index**

Circuits and Systems II: Analog and Digital Signal Processing, IEEE

Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 46 , Issue: 12 , Dec. 1999
Pages:7 - 26

[Abstract] [PDF Full-Text (284 KB)] **IEEE JNL**

---

25 **IEEE standard for integrated circuit (IC) delay and power calculation system**

IEEE Std 1481-1999 , 26 June 1999
Pages:i - 390

[Abstract] [PDF Full-Text (1780 KB)] **IEEE STD**

---

26 **C-based SoC design flow and EDA tools: an ASIC and system vendor perspective**
Wakabayashi, K.; Okamoto, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 19 , Issue: 12 , Dec. 2000
Pages:1507 - 1522

[Abstract] [PDF Full-Text (388 KB)] **IEEE JNL**

---

27 **An industrial view of electronic design automation**
MacMillen, D.; Camposano, R.; Hill, D.; Williams, T.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 19 , Issue: 12 , Dec. 2000
Pages:1428 - 1448

[Abstract] [PDF Full-Text (180 KB)] **IEEE JNL**

---

28 **Designing electronic engines with electronic engines: 40 years of bootstrapping of a technology upon itself**
Jess, J.A.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 19 , Issue: 12 , Dec. 2000
Pages:1404 - 1427

[Abstract] [PDF Full-Text (280 KB)] **IEEE JNL**

---

29 **Computer-aided design of analog and mixed-signal integrated circuits**
Gielen, G.G.E.; Rutenbar, R.A.;
Proceedings of the IEEE , Volume: 88 , Issue: 12 , Dec. 2000
Pages:1825 - 1854

[Abstract] [PDF Full-Text (552 KB)] **IEEE JNL**

---

30 **IP protection of DSP algorithms for system on chip implementation**
Chapman, R.; Durrani, T.S.;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on] , Volume: 48 , Issue: 3 , March 2000

Pages:854 - 861

[Abstract] [PDF Full-Text (176 KB)] **IEEE JNL**

---

31 **A microprocessor design project in an introductory VLSI course**
Brown, R.B.; Lomax, R.J.; Carichner, G.; Drake, A.J.;
Education, IEEE Transactions on , Volume: 43 , Issue: 3 , Aug. 2000
Pages:353 - 361

[Abstract] [PDF Full-Text (524 KB)] **IEEE JNL**

---

32 **PROTEUS-Lite project: dedicated to developing a telecommunication-oriented FPGA and its applications**
Miyazaki, T.; Takahara, A.; Murooka, T.; Katayama, M.; Ichimori, T.; Shirakawa, K.; Tsutsui, A.; Fukami, K.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 8 , Issue: 4 , Aug. 2000
Pages:401 - 414

[Abstract] [PDF Full-Text (632 KB)] **IEEE JNL**

---

33 **A 30-frames/s megapixel real-time CMOS image processor**
Doswald, D.; Hafliger, J.; Blessing, P.; Felber, N.; Niederer, P.; Fichtner, W.;
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 11 , Nov. 2000
Pages:1732 - 1743

[Abstract] [PDF Full-Text (320 KB)] **IEEE JNL**

---

34 **System design consideration for digital wheelchair controller**
Ruei-Xi Chen; Liang-Gee Chen; Lilin Chen;
Industrial Electronics, IEEE Transactions on , Volume: 47 , Issue: 4 , Aug. 2000
Pages:898 - 907

[Abstract] [PDF Full-Text (1496 KB)] **IEEE JNL**

---

35 **Rapid prototyping using field-programmable logic devices**
Hamblen, J.O.;
Micro, IEEE , Volume: 20 , Issue: 3 , May-June 2000
Pages:29 - 37

[Abstract] [PDF Full-Text (1536 KB)] **IEEE JNL**

---

36 **A new qualitative metric for assessing advanced graduate courses in computer engineering and science**
Ghosh, S.;
Circuits and Devices Magazine, IEEE , Volume: 16 , Issue: 6 , Nov. 2000
Pages:11 - 20

[Abstract] [PDF Full-Text (204 KB)] **IEEE JNL**

---

37 **Limitations and challenges of computer-aided design technology for CMOS VLSI**
Bryant, R.E.; Kwang-Ting Cheng; Kahng, A.B.; Keutzer, K.; Maly, W.; Newton, R.; Pileggi, L.; Rabaey, J.M.; Sangiovanni-Vincentelli, A.;
Proceedings of the IEEE , Volume: 89 , Issue: 3 , March 2001
Pages:341 - 365

[Abstract] [PDF Full-Text (272 KB)] **IEEE JNL**

---

38 **Quantitative study of the impact of design and synthesis options on processor core performance**
Bautista, T.; Nunez, A.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 3 , June 2001
Pages:461 - 473

[Abstract] [PDF Full-Text (316 KB)] **IEEE JNL**

---

39 **An efficient architecture for two-dimensional discrete wavelet transform**
Po-Cheng Wu; Liang-Gee Chen;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 11 , Issue: 4 , April 2001
Pages:536 - 545

[Abstract] [PDF Full-Text (644 KB)] **IEEE JNL**

---

40 **Activity-driven clock design**
Farrahi, A.H.; Chunhong Chen; Srivastava, A.; Tellez, G.; Sarrafzadeh, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 , Issue: 6 , June 2001
Pages:705 - 714

[Abstract] [PDF Full-Text (216 KB)] **IEEE JNL**

---

41 **A new contactless smart card IC using an on-chip antenna and an asynchronous microcontroller**
Abrial, A.; Bouvier, J.; Renaudin, M.; Senn, P.; Vivet, P.;
Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 7 , July 2001
Pages:1101 - 1107

[Abstract] [PDF Full-Text (128 KB)] **IEEE JNL**

---

42 **80-Mb/s QPSK and 72-Mb/s 64-QAM flexible and scalable digital OFDM transceiver ASICs for wireless local area networks in the 5-GHz band**
Eberle, W.; Derudder, V.; Vanwijnsberghe, G.; Vergara, M.; Deneire, L.; Van der Perre, L.; Engels, M.G.E.; Bolsens, I.; De Man, H.;
Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 11 , Nov. 2001
Pages:1829 - 1838

[Abstract] [PDF Full-Text (333 KB)] **IEEE JNL**

---

43 **Software implementation of synchronous programs**
Andre, C.; Boulanger, F.; Girault, A.;
Application of Concurrency to System Design, 2001. Proceedings. 2001 International Conference on , 25-29 June 2001
Pages:133 - 142

[Abstract] [PDF Full-Text (238 KB)] **IEEE CNF**

---

44 **IEEE standard Verilog hardware description language**

IEEE Std 1364-2001 , 2001
Pages:0_1 - 856

[Abstract] [PDF Full-Text (3773 KB)] **IEEE STD**

---

45 **Chip design of portable speech memopad suitable for persons with visual disabilities**
Jhing-Fa Wang; Jia-Ching Wang; Han-Chiang Chen; Tai-Lung Chen; Chin-Chan Chang; Ming-Chi Shih;
Speech and Audio Processing, IEEE Transactions on , Volume: 10 , Issue: 8 , Nov. 2002
Pages:644 - 658

[Abstract] [PDF Full-Text (1226 KB)] **IEEE JNL**

---

46 **A "flying-adder" architecture of frequency and phase synthesis with scalability**
Liming Xiu; Zhihong You;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 5 , Oct. 2002
Pages:637 - 649

[Abstract] [PDF Full-Text (680 KB)] **IEEE JNL**

---

47 **FPGA realization of wavelet transform for detection of electric power system disturbances**
Shyh-Jier Huang; Tsai-Ming Yang; Jiann-Tseng Huang;
Power Delivery, IEEE Transactions on , Volume: 17 , Issue: 2 , April 2002
Pages:388 - 394

[Abstract] [PDF Full-Text (346 KB)] **IEEE JNL**

---

48 **An introductory digital design course using a low-cost autonomous robot**
Newman, K.E.; Hamblen, J.O.; Hall, T.S.;
Education, IEEE Transactions on , Volume: 45 , Issue: 3 , Aug. 2002
Pages:289 - 296

[Abstract] [PDF Full-Text (308 KB)] **IEEE JNL**

---

49 **Performance characterization of FPGA techniques for calibration and beamforming in smart antenna applications**
Nuteson, T.W.; Stocker, J.E.; Clark, J.S.; Haque, D.S.; Mitchell, G.S.;
Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue: 12 , Dec. 2002
Pages:3043 - 3051

[Abstract] [PDF Full-Text (859 KB)] **IEEE JNL**

---

50 **Minimizing memory access energy in embedded systems by selective instruction compression**
Benini, L.; Macii, A.; Macii, E.; Poncino, M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 5 , Oct. 2002
Pages:521 - 531

[Abstract] [PDF Full-Text (793 KB)] **IEEE JNL**

1 2 3 Next

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **8** of **1128145** documents.
A maximum of **500** results are displayed, **50** to a page, sorted by **Publication year** in **Ascending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

clock and control and hdl Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Hardware implementation of a multiprocessor system controlled by Petri nets**
Anzai, F.; Kawahara, N.; Takei, T.; Watanabe, T.; Murakoshi, H.; Kondo, T.; Dohi, Y.;
Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on , 15-19 Nov. 1993
Pages:121 - 126 vol.1

[Abstract] [PDF Full-Text (372 KB)] **IEEE CNF**

---

2 **A synthesis method for mixed synchronous/asynchronous behavior**
Tsung-Yi Wu; Tzu-Chie Tien; Wu, A.C.-H.; Youn-Long Lin;
European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings. , 28 Feb.-3 March 1994
Pages:277 - 281

[Abstract] [PDF Full-Text (436 KB)] **IEEE CNF**

---

3 **Autocircuit: a clock edge general behavioral synthesis system with a direct path to physical datapaths**
Ugurdag, H.F.; Fuhrman, T.E.;
Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceedings., 1996 IEEE International Conference on , 7-9 Oct. 1996
Pages:514 - 523

[Abstract] [PDF Full-Text (1072 KB)] **IEEE CNF**

---

4 **Precision and performance of numerically controlled oscillators with hybrid function generators**
Janiszewski, I.; Hoppe, B.; Meuth, H.;
Frequency Control Symposium and PDA Exhibition, 2001. Proceedings of the

2001 IEEE International , 6-8 June 2001
Pages:744 - 752

[Abstract] [PDF Full-Text (768 KB)] **IEEE CNF**

---

5 **Numerically controlled oscillators with hybrid function generators**
Janiszewski, I.; Hoppe, B.; Meuth, H.;
Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on , Volume: 49 , Issue: 7 , July 2002
Pages:995 - 1004

[Abstract] [PDF Full-Text (1097 KB)] **IEEE JNL**

---

6 **HDL synthesis and simulation of eight bit DSP based micro-controller for image processing applications**
Rangarajan, P.; Kutraleeshwaran, V.; Vaasanthy, K.; Perinbam, R.P.;
Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 3 , 4-7 Aug. 2002
Pages:III - 609-12 vol.3

[Abstract] [PDF Full-Text (282 KB)] **IEEE CNF**

---

7 **Low cost floating point arithmetic unit design**
Seungchul Kim; Yongjoo Lee; Wookyeong Jeong; Yongsurk Lee;
ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on , 6-8 Aug. 2002
Pages:217 - 220

[Abstract] [PDF Full-Text (330 KB)] **IEEE CNF**

---

8 **A low-cost digital controller for a switching DC converter with improved voltage regulation**
Islam, M.M.; Allee, D.R.; Konasani, S.; Rodriguez, A.A.;
Power Electronics Letters, IEEE , Volume: 2 , Issue: 4 , Dec. 2004
Pages:121 - 124

[Abstract] [PDF Full-Text (216 KB)] **IEEE JNL**
